REMARKS/ARGUMENTS

The Examiner is thanked for the thorough examination and search of the subject.

Claims 242-248 and 250-274 are pending; Claims 242-245, 247, 248, 250-252, 254, 256, 257, 259-264, 266, 268-271 and 273 have been currently amended; Claims 253, 255, 265, 267, 272 and 274 have been withdrawn and currently amended; Claims 1-241 and 249 have been canceled.

Response to Claim Rejections under 35 U.S.C. 102 and 103

Applicants respectfully traverse the rejections for at least the reasons set forth below.

Response to Claims 242, 245-248 and 250-256

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As currently amended, independent Claim 242 is recited below:

242. A method for fabricating a chip package comprising:

joining a die and a substrate, said die having a top surface at horizontal level, wherein said die and said substrate are under said horizontal level;

after said joining said die and said substrate, forming a patterned circuit layer over said horizontal level, said patterned circuit layer extending across an edge of said die;

after said joining said die and said substrate, forming a passive device over said horizontal level, wherein said passive device is entirely not directly over said die; and

separating said substrate into multiple portions.

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Section I

Reconsiderations of Claims 242, 245, 249, 250, 252, 254 and 256 rejected under 35 U.S.C. 102(e) as being anticipated by Towle et al. (U.S. Pub. 2002/0074641), of Claims 251 and 253 rejected under 35 U.S.C. 103(a) as being unpatentable over by Towle et al. in view of Stamper et al. (U.S. Pat. 6,331,481), and of Claim 255 rejected under 35 U.S.C. 103(a) as being unpatentable over by Towle et al. in view of Shoji (U.S. Pub. 2001/0013653) are requested in accordance with the following remarks.

Applicants respectfully assert that the method claimed in Claim 242 patentably distinguishes over the citation by Towle et al. (U.S. Pub. 2002/0074641).

Towle et al. teach that a method comprises depositing multiple patterned circuit layers 114, 114', 114", 116, 116", 120 and 120' and multiple insulating layers 104, 104' and 104" over the substrate 202. *~ See FIGS. 1-8 and 11-19, Pars. 0023-0025, and Par. 0032, lines 1-3 ~* The laminated interconnector 130 having the patterned circuit layers 114, 114', 114", 116, 116", 120 and 120' and the insulating layers 104, 104' and 104" therebetween creates resistance, capacitance and inductance, but Towle et al. fail to teach, hint or suggest that the resistance, capacitance or inductance can be used for a resistor, capacitor or inductor, namely, a passive device. The Examiner would not focus too much on whether a structure having multiple patterned circuit layers and multiple insulating layers therebetween is disclosed or not, but instead reconsider the functional limitation. A functional limitation should be evaluated and considered, just like any other limitation of the claim. *~ See MPEP 2173.05(g) ~*

The Examiner considers that "With respect to Towle applicant contends that

examiner should evaluate the function. Examiner agree and has been considered. However, because the prior art discloses the structure as claimed, it is capable of performing the same function as indicated above". *~ See point 34 in page 11, in the last Office Action mailed May 21, 2007 ~*

Applicants respectfully traverse the Examiner's opinion. Towle et al. fail to teach the claimed subject matter of forming a passive device over a substrate and over a horizontal level defined by a top surface of a die. The prior art does not disclose the structure, passive device, as claimed. The laminated interconnector 130 having the patterned circuit layers 114, 114', 114'', 116, 116'', 120 and 120' and the insulating layers 104, 104' and 104'' therebetween can not be deemed with a passive device because the resistance, capacitance or inductance created by the laminated interconnector 130 is not used for a resistor, capacitor or inductor, namely, a passive device.

Withdrawal of Rejection under 35 U.S.C. 102(e) to Claim 242 is respectfully requested.

For at least the foregoing reasons, applicants respectfully submit independent Claim 242 patently distinguishes over the prior art references, and should be allowed. For at least the same reasons, dependent Claims 245-248 and 250-256 patently define over the prior art as well.

Section II

Reconsiderations of Claims 242, 245, 246 and 254-256 rejected under 35 U.S.C. 103(a) as being unpatentable over Sakamoto et al. (U.S. Pub. 2002/0133943) are requested in accordance with the following remarks.

Applicants respectfully assert that the method claimed in Claim 242 patentably distinguishes over the citation by Sakamoto et al. (U.S. Pub. 2002/0133943).

Sakamoto et al. fail to teach, hint or suggest the subject matter of forming a patterned circuit layer over a horizontal level defined by a top surface of a die, said patterned circuit layer extending across an edge of said die, as claimed in currently amended Claim 242.

Withdrawal of Rejection under 35 U.S.C. 103(a) to Claim 242 is respectfully requested.

For at least the foregoing reasons, applicants respectfully submit independent Claim 242 patently distinguishes over the prior art references, and should be allowed. For at least the same reasons, dependent Claims 245-248 and 250-256 patently define over the prior art as well.

Section III

Reconsiderations of Claim 242 rejected under 35 U.S.C. 103(a) as being unpatentable over Tabrizi (U.S. Pat. 6,867,499) are requested in accordance with the following remarks.

Applicants respectfully assert that the method claimed in Claim 242 patentably distinguishes over the citation by Tabrizi (U.S. Pat. 6,867,499).

Tabrizi teaches that a chip packaging method comprises joining a die 520 and a substrate 510, and separating the substrate 510. ~ *See FIG. 5 and col. 4, lines 9-13* ~ Tabrizi teaches that a passive device may be added for the chip package. ~ *See col. 5,*

lines 1-4 ~ However, Tabrizi fails to teach or show where is the exact place of the chip package having a passive device formed thereover. Tabrizi fails to teach, hint or suggest there may be a passive device over a substrate, but not directly over a die, as claimed in Claim 242.

The Examiner considers that "since placement of a capacitor to either the left or right of die would not modify the operation of the device and applicant has not disclosed that the placement is for any unobvious or critical reasons, the rearrangement of the capacitor would have been obvious since it has been held that the mere shifting of parts without providing modification to the device is obvious". ~ *See point 27, in page 9, in the last Office Action mailed May 21, 2007* ~

Applicants respectfully traverse the Examiner's opinions. The placement of a passive device entirely not directly over a die leads the passive device far away from the die, and thereby the interference between the passive device and the die can be reduced, which is not anticipated by Tabrizi, in contrast to the placement of depositing a passive device directly over a die. As a result, the placement of a passive device entirely formed not directly over a die modifies the operation of the chip structure.

In response to point 33 in pages 10 and 11, in the Office Action mailed May 21, 2007, Claim 242 has been currently amended with the subject matter that "said passive device is entirely not directly over said die", which is believed that the Examiner's argument has been overcome.

Withdrawal of Rejection under 35 U.S.C. 103(a) to Claim 242 is respectfully requested.

For at least the foregoing reasons, applicants respectfully submit independent

Claim 242 patently distinguishes over the prior art references, and should be allowed. For at least the same reasons, dependent Claims 245-248 and 250-256 patently define over the prior art as well.

Response to Claims 243 and 257-268

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As currently amended, independent Claim 243 is recited below:

243. A method for fabricating a chip package comprising:

joining a die and a substrate, said die having a top surface at horizontal level, wherein said die and said substrate are under said horizontal level;

after said joining said die and said substrate, forming a passive device over said horizontal level, said passive device having a first connection point connected to said die;

after said forming said passive device, forming a metal bump over said horizontal level, wherein said metal bump is connected to a second connection point of said passive device; and

separating said substrate into multiple portions.

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Section I

Reconsiderations of Claims 243, 257, 261, 262, 264, 266 and 268 rejected under 35 U.S.C. 102(e) as being anticipated by Towle et al. (U.S. Pub. 2002/0074641), of Claim 263 and 265 rejected under 35 U.S.C. 103(a) as being unpatentable over by Towle et al. in view of Stamper et al. (U.S. Pat. 6,331,481), and of Claim 267 rejected under 35 U.S.C. 103(a) as being unpatentable over by Towle et al. in view of Shoji (U.S. Pub. 2001/0013653) are requested in accordance with the following remarks.

Applicants respectfully assert that the method claimed in Claim 243 patentably distinguishes over the citation by Towle et al. (U.S. Pub. 2002/0074641).

Towle et al. teach that a method comprises depositing multiple patterned circuit layers 114, 114', 114", 116, 116", 120 and 120' and multiple insulating layers 104, 104' and 104" over the substrate 202. ~ *See FIGS. 1-8 and 11-19, Pars. 0023-0025, and Par. 0032, lines 1-3* ~ The laminated interconnector 130 having the patterned circuit layers 114, 114', 114", 116, 116", 120 and 120' and the insulating layers 104, 104' and 104" therebetween creates resistance, capacitance and inductance, but Towle et al. fail to teach, hint or suggest that the resistance, capacitance or inductance can be used for a resistor, capacitor or inductor, namely, a passive device. The Examiner would not focus too much on whether a structure having multiple patterned circuit layers and multiple insulating layers therebetween is disclosed or not, but instead reconsider the functional limitation. A functional limitation should be evaluated and considered, just like any other limitation of the claim. ~ *See MPEP 2173.05(g)* ~

The Examiner considers that "With respect to Towle applicant contends that examiner should evaluate the function. Examiner agree and has been considered. However, because the prior art discloses the structure as claimed, it is capable of performing the same function as indicated above". ~ *See point 34 in page 11, in the last Office Action mailed May 21, 2007* ~

Applicants respectfully traverse the Examiner's opinion. Towle et al. fail to teach the claimed subject matter of forming a passive device over a substrate and over a horizontal level defined by a top surface of a die. The prior art does not disclose the structure, passive device, as claimed. The laminated interconnector 130 having the patterned circuit layers 114, 114', 114", 116, 116", 120 and 120' and the insulating layers

104, 104' and 104'' therebetween can not be deemed with a passive device because the resistance, capacitance or inductance created by the laminated interconnector 130 is not used for a resistor, capacitor or inductor, namely, a passive device.

Withdrawal of Rejection under 35 U.S.C. 102(e) to Claim 243 is respectfully requested.

For at least the foregoing reasons, applicants respectfully submit independent Claim 243 patently distinguishes over the prior art references, and should be allowed. For at least the same reasons, dependent Claims 257-268 patently define over the prior art as well.

Section II

Reconsiderations of Claims 243, 257, 258 and 266-268 rejected under 35 U.S.C. 103(a) as being unpatentable over Sakamoto et al. (U.S. Pub. 2002/0133943) are requested in accordance with the following remarks.

Applicants respectfully assert that the method claimed in Claim 243 patentably distinguishes over the citation by Sakamoto et al. (U.S. Pub. 2002/0133943).

Sakamoto et al. fail to teach, hint or suggest the subject matters of forming a patterned circuit layer over a horizontal level under which a die and a substrate exist, and of forming a metal bump over said horizontal level, as claimed in currently amended Claim 243.

Withdrawal of Rejection under 35 U.S.C. 103(a) to Claim 243 is respectfully requested.

For at least the foregoing reasons, applicants respectfully submit independent Claim 243 patently distinguishes over the prior art references, and should be allowed. For at least the same reasons, dependent Claims 257-268 patently define over the prior art as well.

Section III

Reconsiderations of Claim 243 rejected under 35 U.S.C. 103(a) as being unpatentable over Tabrizi (U.S. Pat. 6,867,499) are requested in accordance with the following remarks.

Applicants respectfully assert that the method claimed in Claim 242 patentably distinguishes over the citation by Tabrizi (U.S. Pat. 6,867,499).

Tabrizi teaches that a chip packaging method comprises joining a die 520 and a substrate 510, and separating the substrate 510. ~ *See FIG. 5 and col. 4, lines 9-13* ~ Tabrizi teaches that a passive device may be added for the chip package. ~ *See col. 5, lines 1-4* ~ However, Tabrizi fails to teach or show what is the connection for the passive device. Tabrizi fails to teach, hint or suggest there may be a passive device having a first connection point connected to a die and a second connection point connected to a metal bump, as claimed in Claim 243.

Withdrawal of Rejection under 35 U.S.C. 103(a) to Claim 243 is respectfully requested.

For at least the foregoing reasons, applicants respectfully submit independent Claim 243 patently distinguishes over the prior art references, and should be allowed.

For at least the same reasons, dependent Claims 257-268 patently define over the prior art as well.

Response to Claims 244 and 269-274

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As currently amended, independent Claim 244 is recited below:

244. A method for fabricating a chip package comprising:

providing a first die having a first top surface at a horizontal level;

providing a second die having a second top surface at said horizontal level;

forming a passive device over said horizontal level, wherein said passive device is entirely not directly over said first and second dies;

after said forming said passive device over said horizontal level, forming an insulating layer on said passive device; and

forming a patterned circuit layer over said horizontal level, wherein said patterned circuit layer extends across an edge of said first die.

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Section I

Reconsiderations of Claims 244 and 269 rejected under 35 U.S.C. 102(e) as being anticipated by Nuytkens et al. (U.S. Pat. 6,838,750), and of Claims 273 and 274 rejected under 35 U.S.C. 103(a) as being unpatentable over Nuytkens et al. are requested in accordance with the following remarks.

Applicants respectfully assert that the method claimed in Claim 244 patentably distinguishes over the citation by Nuytkens et al. (U.S. Pat. 6,838,750).

Nuytkens et al. teach that multiple passive devices 146 and 148 are formed over a chip package. However, Nuytkens et al. fail to teach, hint or suggest that there may be an insulating layer formed on the passive devices 146 and 148, as claimed in Claim 244.

Withdrawal of Rejection under 35 U.S.C. 102(e) to Claim 244 is respectfully requested.

For at least the foregoing reasons, applicants respectfully submit independent Claim 244 patently distinguishes over the prior art references, and should be allowed. For at least the same reasons, dependent Claims 269-274 patently define over the prior art as well.

Section II

Reconsiderations of Claims 244, 269, 271 and 273 rejected under 35 U.S.C. 102(e) as being anticipated by Towle et al. (U.S. Pub. 2002/0074641), of Claim 270 and 272 rejected under 35 U.S.C. 103(a) as being unpatentable over by Towle et al. in view of Stamper et al. (U.S. Pat. 6,331,481), and of Claim 274 rejected under 35 U.S.C. 103(a) as being unpatentable over by Towle et al. in view of Shoji (U.S. Pub. 2001/0013653) are requested in accordance with the following remarks.

Applicants respectfully assert that the method claimed in Claim 244 patentably distinguishes over the citation by Towle et al. (U.S. Pub. 2002/0074641).

Towle et al. teach that a method comprises depositing multiple patterned circuit layers 114, 114', 114", 116, 116", 120 and 120' and multiple insulating layers 104, 104' and 104" over the substrate 202. *~ See FIGS. 1-8 and 11-19, Pars. 0023-0025, and Par. 0032, lines 1-3 ~* The laminated interconnector 130 having the patterned circuit layers

114, 114', 114", 116, 116", 120 and 120' and the insulating layers 104, 104' and 104" therebetween creates resistance, capacitance and inductance, but Towle et al. fail to teach, hint or suggest that the resistance, capacitance or inductance can be used for a resistor, capacitor or inductor, namely, a passive device. The Examiner would not focus too much on whether a structure having multiple patterned circuit layers and multiple insulating layers therebetween is disclosed or not, but instead reconsider the functional limitation. A functional limitation should be evaluated and considered, just like any other limitation of the claim. *~ See MPEP 2173.05(g) ~*

The Examiner considers that "With respect to Towle applicant contends that examiner should evaluate the function. Examiner agree and has been considered. However, because the prior art discloses the structure as claimed, it is capable of performing the same function as indicated above". *~ See point 34 in page 11, in the last Office Action mailed May 21, 2007 ~*

Applicants respectfully traverse the Examiner's opinion. Towle et al. fail to teach the claimed subject matter of forming a passive device over a substrate and over a horizontal level defined by a top surface of a die. The prior art does not disclose the structure, passive device, as claimed. The laminated interconnector 130 having the patterned circuit layers 114, 114', 114", 116, 116", 120 and 120' and the insulating layers 104, 104' and 104" therebetween can not be deemed with a passive device because the resistance, capacitance or inductance created by the laminated interconnector 130 is not used for a resistor, capacitor or inductor, namely, a passive device.

Withdrawal of Rejection under 35 U.S.C. 102(e) to Claim 244 is respectfully requested.

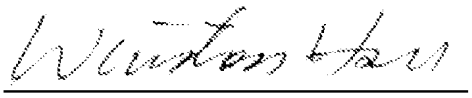
For at least the foregoing reasons, applicants respectfully submit independent

Claim 244 patently distinguishes over the prior art references, and should be allowed. For at least the same reasons, dependent Claims 269-274 patently define over the prior art as well.

CONCLUSION

Some or all of the pending claims are believed to be in condition for Allowance, and that is so requested.

Sincerely yours,



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Winston Hsu, Patent Agent No. 41,526
P.O. BOX 506, Merrifield, VA 22116, U.S.A.
Voice Mail: 302-729-1562
Facsimile: 806-498-6673
e-mail : winstonhsu@naipo.com

Note: Please leave a message in my voice mail if you need to talk to me. (The time in D.C. is 12 hours behind the Taiwan time, i.e. 9 AM in D.C. = 9 PM in Taiwan.)